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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/020,647	FJELSTAD ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 45-49, 51, 52 and 54-57 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The undescribed subject matter is the claim 45 limitation, "before providing the compliant layer, plating a barrier metal atop the contacts of said semiconductor chip."

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered

therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 35-38, 40, 41, 45-54 and 57 are rejected under 35 U.S.C. 102(b) as anticipated by Kwon (5070297) or, in the alternative, under 35 U.S.C. 103(a) as obvious over the combination of Kwon (5070297) and Chen (4671849).

At column 4, line 13 to column 7, line 62, Kwon teaches the following:

35. A method of making a compliant semiconductor chip package comprising: providing a semiconductor chip 14 having a contact bearing surface including a central region bounded by a peripheral region, wherein the peripheral region of said contact bearing surface has chip contacts 36; providing a dielectric protective layer 34 over the contact bearing surface of said semiconductor chip, said dielectric protective layer having apertures for said chip contacts;

providing a compliant layer 32 over said dielectric protective layer and over the central region of the contact bearing face of

said semiconductor chip, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to said dielectric protective layer and sloping edges between the top surface and the bottom surface, wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said compliant layer; and selectively electroplating elongated bond ribbons 28 atop said dielectric protective layer and said compliant layer, wherein each said bond ribbon electrically connects one of said chip contacts to an associated conductive terminal 20-22-24 disposed on the top surface of said compliant layer, and wherein said elongated bond ribbons extend along the sloping edges of said compliant layer and have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer.

36. The method according to 35, further comprising after selectively electroplating said bond ribbons, providing a second dielectric protective layer 26 over exposed elements 28 on the terminal side of said package, wherein said second dielectric protective layer has a plurality of apertures extending therethrough for providing access to said terminals.

37. The method according to 35, wherein said compliant layer comprises a material selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

38. The method according to 35, further including the step of providing an encapsulant layer 26 atop an exposed surface of said bond ribbons.

40. The method according to 38, further including the step of providing a second dielectric layer 21 atop said encapsulant layer, wherein said second dielectric layer has a plurality of apertures for providing access to said terminals.

41. The method according to 35, wherein said dielectric layer is a silicon dioxide passivation layer provided on the contact bearing surface of said semiconductor chip.

45. A method of making a compliant microelectronic package comprising:

providing a microelectronic element 14 having a first surface and a plurality of contacts disposed on the first surface thereof; providing a compliant layer over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of said microelectronic element, a top surface facing upwardly away from

said microelectronic element and one or more sloping edge surfaces extending between the top and bottom surfaces of said compliant layer, wherein the sloping edges of said compliant layer have first curved transition regions near the top surface of said compliant layer and second curved transition regions near the bottom surface of said compliant layer; and

selectively forming elongated, flexible bond ribbons over the top surface and the sloping edge surfaces of said compliant layer for electrically connecting said contacts to conductive terminals overlying the top surface of said compliant layer, wherein said elongated, flexible bond ribbons extending along the sloping edges of said compliant layer have first curved regions overlying the first curved transition regions of said compliant layer and second curved regions overlying the second curved transition regions of said compliant layer.

46. The method as in 45, wherein the contacts are disposed in a first region of the first surface of said microelectronic element, and said compliant layer overlies a second region of the first surface of said microelectronic element, and wherein the sloping edges of said

compliant layer extend along one or more borders between the first and second regions of the first surface of said microelectronic element.

47. The method as in 45, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

48. The method as claimed in 45, wherein said selectively forming bond ribbons step includes depositing a conductive material over the top of said package and etching away portions of said conductive material.

49. The method as in 45, further comprising:

before the providing a compliant layer step, providing a first dielectric protective layer over the first surface of said microelectronic element, the first dielectric layer having a plurality of apertures in substantial alignment with said contacts for providing access to said contacts, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

50. The method as in 49, the selectively forming flexible bond ribbons step including electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

51. The method as in 45, further including the step of providing a dielectric cover layer 26 over said compliant layer and said bond ribbons after the step of selectively forming said bond ribbons, wherein said dielectric cover layer has a plurality of apertures for accessing said terminals therethrough.

52. The method as in 45, further including the step of providing an encapsulant layer 26 over an exposed surface of said bond ribbons.

53. The method as in 52, further including the step of providing a second dielectric protective layer 21 atop the encapsulant layer, wherein the second dielectric protective layer has a plurality of apertures for accessing said terminals therethrough.

54. The method as in 45, further including before the step of forming said bond ribbons, depositing a barrier metal 30 atop said contacts, wherein said barrier metal inherently minimizes voiding between said contacts and said bond ribbons.

57. The method as in 45, wherein the sloping edge surfaces of said compliant layer extend in both vertical and horizontal directions.

To further clarify the teaching of forming elongated bond ribbons 28, it is noted that Kwon teaches that the contacts 28 are small and narrow in width in proportion to length or height; therefore, the contacts are elongated.

To further clarify the teaching of first transition regions near the top surface of the compliant layer and second transition regions near the bottom surface of the compliant layer, it is noted that it is inherent that the first and second

regions near the top and bottom surface, respectively, transition into neighboring regions of the compliant layer and other neighboring layers.

To further clarify the teaching wherein the sloping edges of the compliant layer have a first curved transition region near the top surface of the compliant layer and a second curved transition region near the bottom surface of the compliant layer, and the elongated bond ribbons have a first curved region overlying the first curved transition region of the compliant layer and a second curved region overlying the second curved transition region of the compliant layer, it is noted that the sloping edges of the compliant layer have a first straight line transition region near the top surface of the compliant layer and a second straight line transition region near the bottom surface of the compliant layer, and the elongated bond ribbons have a first straight line region overlying the first transition region of the compliant layer and a second straight line region overlying the second transition region of the compliant layer. In addition, a curved region comprises a line defined by an equation so that the coordinates of its points are functions of a single independent variable or parameter. Furthermore, a straight line is defined by an equation so that the coordinates of its points are functions of a single independent variable or

parameter; namely, the equation $y = mx + b$. Therefore, the straight line regions of Kwon are curved.

Because applicant appears to have introduced the claimed limitations, "wherein the sloping edges of said compliant layer have a first curved transition region near the top surface of said compliant layer and a second curved transition region near the bottom surface of said compliant layer," and, "wherein said elongated bond ribbons . . . have a first curved region overlying the first curved transition region of said compliant layer and a second curved region overlying the second curved transition region of said compliant layer," primarily in order to overcome a rejection over Kwon, in the alternative, the claims are further rejected under 35 U.S.C. 103(a) as obvious over the combination of Kwon (5070297) and Chen (4671849).

Specifically, Kwon does not appear to explicitly teach curved transition regions. Nonetheless, at column 1, lines 10-13; and column 3, lines 52-64, Chen explicitly teaches curved transition regions. Moreover, it would have been obvious to combine the process of Chen with the process of Kwon because it would minimize defects in the bond ribbons.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon or the combination of Kwon and Chen as

applied to claims 35-38, 40, 41, 45-54 and 57, and further in combination with LeGrange (4962985).

Kwon or the combination of Kwon and Chen does not appear to explicitly teach the following:

39. The method according to 38, wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

Nonetheless, at column 1, lines 26-34, LeGrange teaches a process comprising a silicone encapsulation layer.

In addition, it would have been obvious to combine the process of LeGrange with the process of the applied prior art because it would provide an encapsulation layer.

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon or the combination of Kwon and Chen as applied to claims 35-38, 40, 41, 45-54 and 57, and further in combination with Chikawa (5310699).

Although, as cited, Kwon teaches plating a barrier metal atop the contacts, Kwon or the combination of Kwon and Chen does not appear to explicitly teach plating before providing the compliant layer.

Notwithstanding, at column 5, lines 5-10, Chikawa teaches plating 6′ a contact 5 before applying a compliant layer 9.

Moreover, it would have been obvious to combine the process of Chikawa with the process of the applied prior art because it would prevent diffusion.

Claims 43, 44, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon as applied to claims 35-38, 40, 41, 45-54 and 57, and further in combination with Palagonia (5874782).

As cited supra, Kwon teaches the following:

43. The method according to 35, wherein the method steps are applied simultaneously to a plurality of undiced semiconductor chips 14 on a wafer 10 to form a plurality of compliant semiconductor chip packages 14.

44. The method according to 35, wherein the method steps are applied simultaneously to a plurality of adjacent semiconductor chips arranged in an array to form a plurality of compliant semiconductor chip packages.

55. The method as in 45, wherein the method is applied to a plurality of undiced semiconductor chips on a wafer to form a plurality of compliant semiconductor chip packages.

56. The method as in 45, wherein the method is applied to a plurality of adjacent semiconductor chips arranged in an array to form a corresponding plurality of compliant semiconductor chip packages.

However, Kwon does not appear to explicitly teach dicing said wafer after selectively electroplating said bond ribbons to provide a plurality of individual compliant semiconductor chip packages, separating the packages after the selectively forming elongated, flexible bonds ribbons step, and separating the plurality of compliant semiconductor chip packages from one another following the step of selectively electroplating the bond ribbons.

Nevertheless, at column 1, lines 1-56; column 5, line 64 to column 6, line 6; and column 6, lines 21-39, Palagonia teaches dicing a wafer 20 after selectively electroplating bond ribbons 26 to provide a plurality of individual compliant semiconductor chip packages 22, separating packages after a selectively forming elongated, flexible bonds ribbons step, and separating the plurality of compliant semiconductor chip packages from one another following the step of selectively electroplating the bond ribbons. In addition, it would have been obvious to combine the process of Palagonia with the process of the applied prior art because it would facilitate testing of individual chips.

Applicant's remarks filed 4-23-02 have been fully considered and are adequately addressed in the rejection supra and elsewhere in the record.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/308-7722.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
12-Jul-02